REMARKS/ARGUMENTS

Favorable consideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1-3 and 5-22 are presently pending in this application, Claim 4 having been canceled without prejudice or disclaimer, Claims 1-3 and 8 having been amended and Claims 10-22 having been newly added by the present amendment.

In the outstanding Office Action, Claim 8 was objected to for informalities; Claims 1-9 were rejected under 35 U.S.C. §103(a) as being unpatentable over Azuma (U.S. Patent 6,836,011) in view of Turlik et al. (U.S. Patent 5,325,265), Farooq et al. (U.S. Patent 6,335,210), Ikeda (JP 11-054884), Uchikawa et al. (U.S. Patent 6,531,661), Milkovich et al. (U.S. 6,516,513), and JP 59-000996 (hereinafter "JP '996"); Claims 1, 3, 4 and 6-8 were rejected under 35 U.S.C. §103(a) as being unpatentable over Milkovich et al.; and Claims 2, 5 and 9 were rejected under 35 U.S.C. §103(a) as being unpatentable over Milkovich et al. in view of Uchikawa et al.

Turning now to the merits, Applicants' invention is directed to an interposer that can be provided between a package substrate and an IC chip electrically connected to the package substrate. As discussed in the background section of Applicants' specification, high frequency IC chips are typically made of a brittle porous material that is prone to cracking under thermal stress. Thus, stress defects in the IC chip occur during loading of the substrate with the IC.[1] Applicants' invention is directed to addressing this problem.

Specifically, Applicants' amended Claim 1 recites an interposer configured to be located between a package substrate made of resin and an IC chip. The interposer includes an insulating base material, wherein a Young's modulus of the insulation base material is 55

[1] US Patent Publication No. 2006/0202322 (Applicants specification) at paragraph 4.

to 440GPa and a thickness of the insulation base material is 0.05 to 1.5 times the thickness of the package substrate. Also recited is a plurality of through holes provided through the insulating base material, at least one of the through holes having formed therein a through hole conductor for connecting the package substrate with the IC chip, wherein the plurality of through holes in the insulating base material are arranged in the form of a grid. New Claim 11 also recites these features with respect to a staggard arrangement of the through holes.

Thus, Applicants amended Claims 1 and 10 clarify that a "Young's modulus of insulation base material is 55 to 440Gpa and a thickness of the insulating base material is 0.05 to 1.5 times the thickness of the package substrate." In contrast, the cited reference to Azuma shows interposer 2 between mother board 3 and IC chip 11. This reference discloses that the thermal expansion coefficients of the interposer 2 and the mother board 3 are adjusted to be almost the same value. However, Azuma is completely silent with respect to the Young's modulus and thickness of the interposer 2. Milkovich et al. discloses an interposer having a three layer structure, the upper layer 3 having the CTE of 5ppm/°C and the elasticity rate of 53Mpsi (3600Pa). But Milkovich et al. never mentions the thickness of the base plate. Similarly, Farooq et al. discloses ceramic base plate 20 having Young's modulus of 50GPa between chip 10 and base member 30, and Turlik et al. shows base member 15 made from SiC, which the Office Action cites as the interposer, for adjusting the thermal expansion coefficient of chip 10 and for ensuring mechanical strength. Also, Turlik et al's base member 15 has a Young's modulus of 410GPa. However Farooq et al. and Turlik et al. never mention the thickness of the base plate. The remaining cited references are cited for teachings in the dependent claims and cannot correct the deficiencies of Azuma, Milkovich, Faroop and Turlik noted above.

Thus, none of the cited references disclose that the "thickness of the insulating base material is 0.05 to 1.5 times the thickness of the package substrate." Nevertheless, the outstanding Office Action states that,

> "[the claimed thickness range] seems so wide as to be readily met by most systems and is also met by Azuma as depicted.
>
> ...Since figs [of Milkovich et al.,] are not to scale interposer 3 thickness not clearly disclosed however since [the thickness] range is very wide it seems obvious that in normal production, interposer 3 thickness would be in recited range especially since lower limit would result in interposer too thin to produce necessary flexibility to avoid damage to solder attachments. This would also be to provide strength to the interposer.[2]

As seen from the above-quoted text, the Office Action apparently acknowledges that the claimed thickness range is not explicitly disclosed in the cited references, but concludes that this feature is "depicted" in the drawings or obvious to one skilled in the art due to design and manufacturing considerations. Applicants submit that this is improper. First, as noted above, none of the cited references disclose anything about thickness values of the interposer in relation to the package substrate. Further, none of the cited references disclose scaled drawings by which one could measure and calculate the thickness range based solely on the drawings (and the Office Action makes no attempt to do this). Still further, although, the Office Action explains that any thickness outside the cited range would be "too thin to produce the necessary flexibility to avoid damage to solder attachments," the Office Action does not provide any evidence in support of this finding. Applicants submit that general assertions that the thickness range "is too broad" or fall within "normal production" techniques cannot support a finding that the cited references disclose that the "thickness of the insulating base material is 0.05 to 1.5 times the thickness of the package substrate," as required by Claims 1 and 11.

[2] Outstanding Office Action at items 2 and 3.

Moreover, even assuming that the claimed thickness range can be gleaned from the cited references, there is no reason to combine the claimed interposer thickness range with the claimed Young's modulus range. Applicants submit that it is the present inventors who analyzed thermal stress during loading of the IC onto the substrate under various conditions and discovered a particular advantage to combining the claimed Young's modulus and thickness. Specifically, Applicants' specification states,

> "If the Young's modulus of the insulation base material constituting the interposer is in the range of 55 to 440GPa and the thickness reaches thickness of resin made package substrate x 0.05 or more, the stiffness of the insulation base material constituting the interposer increases because of such a thickness. For the reason, the deformation and warpage generated because the physical property differ between a portion just below the IC and the other portions of the insulation base material constituting the interposer decreases. Therefore, the amounts of IC's deformation and warpage with the interposer decrease, so that no crevice or breaking occurs in the resin of the wiring layer of the IC.
>
> ... On the other hand, if the thickness of the interposer exceeds thickness of package substrate times 1.5, the interposer is not warped. As a result, stress originating from a difference in thermal expansion coefficient between the IC and the interposer is not relaxed in Z direction but concentrates in X-Y direction (the X-Y direction mentioned here means a direction parallel to the surface of the interposer) and crevice or breaking occurs in the resin of the wiring layer of the IC. Further, a demand for thinning is not met because the entire semiconductor device thickens. As other reason, thickening of the insulation base material is not suitable for formation into a fine structure because a small diameter through hole cannot be formed easily."[3]

Thus, the inventors discovered that the combined features of the claimed Young's modulus and the claimed thickness range provide an improved configuration that suppresses deformation of the insulation base material and crevice or breaking in the resin layer of the IC. The cited references do not disclose any importance of the thickness relationship of an interposer to a package substrate, let alone this relationship in combination with the claimed

[3] Applicants' specification at paragraph 24.

thickness range. In view of this, Applicants submit that the Office Action's combination of these features is impermissible hindsight reasoning based on Applicants' disclosure.

Nevertheless, in order to expedite issuance of a patent in this case, independent Claims 1 and 11 further recite,

> "a plurality of through holes provided through the insulating base material, at least one of said through holes having formed therein a through hole conductor for connecting said package substrate with the IC chip,
> wherein the plurality of through holes in the insulating base material are arranged in he form of a grid."

As discussed in Applicants' specification, when the diameter of the through hole is small, the amount of heat generation increases in the through holes because conductor resistance increases. Where the through holes are disposed in the form of the grid (as in Claim 1) or in the staggered fashion (as in Claim 11), "the temperature distribution of the interposer at the time of usage becomes uniform so that no stress concentrates on any specific location thereby the insulation layer of the IC chip being not damaged. Further, the physical property (thermal expansion coefficient, Young's modulus and the like) of the insulation base material just below the IC chip becomes uniform because the through holes are formed uniformly."[4] None of the cited references disclose this additional feature of the through holes being in a grid or staggered arrangement. This provides an additional basis for patentability of Claims 1 and 11 over the cited references.

Thus, independent Claims 1 and 11 patentably define over the cited references. Further, as the remaining pending claims depend from Claims 1 or 11, these claims also patentably define over the cited references. Nevertheless, Applicants have added new dependent claims which further distinguish the claimed invention from the cited prior art.

Specifically, Claims 8 and 17 recite that the diameter of an opening in at least an end face of the through hole is equal to or larger than the diameter of the hole in the center of the

[4] Applicants' specification at paragraph 23.

through hole. As discussed in Applicants' specification, this feature provides advantages of reducing heat and thermal stress in the area of the through hole.[5] Claims 10 and 19 recite that a diameter of the through hole is 125 μm or less. As discussed in Applicants' specification, this size through hole facilitates arrangement of the through holes in a grid or staggered manner.[6] Further, Claims 20 and 21 specify that the a set of said plurality of through holes corresponding to either a power source electrode or ground electrode terminal of the IC chip are arranged in said grid to effect substantially uniform temperature of the interposer. Similarly, Claim 22 recites that the plurality of through holes are arranged at substantially equal distance from each other. As discussed in Applicant's specification, these features further reduce thermal stress on the interposer.[7] Thus, the above dependent claims provide addition bases for patentability over the cited references.

Consequently, in view of the present amendment, no further issues are believed to be outstanding in the present application and the present application is believed to be in condition for allowance. An early and favorable action is therefore respectfully requested.

Respectfully submitted,

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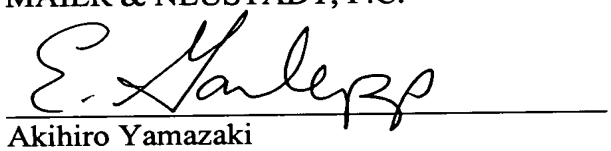

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[5] Applicants' specification at paragraph 24.
[6] Applicants' specification at paragraph 23.
[7] Applicants' specification at paragraph 23.